more correctly determine whether or not the re-communication in the same sector (cell).

What is claimed is:

1. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than a communication stop time interval threshold value on starting of re-communication, said known signal replica generating means making said delay profile calculating means generate a delay profile near to the spreading timing on a previous communication by using only one spreading code stored in said spreading code and spreading timing memory means when said timer value is less than the communication stop time interval threshold value on staring of the re-communication.

2. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by detecting a peak of power values in said delay profiles to produce a spreading code and spreading timing detected signal indicative of the using spreading code and the using spreading timing;

received data processing means, connected to said spreading code and spreading timing detecting means, for carrying out a demodulating processing on the in-phase component signal and the quadrature component signal to produce a demodulated output signal;

spreading code and spreading timing memory means, connected to said spreading code and spreading timing detecting means, for storing information of the using spreading code and the using spreading timing represented by said spreading code and spreading timing detected signal therein, said spreading code and spreading timing memory means producing a spreading code and spreading timing stored signal;

a timer for counting an elapsed time interval from an end of communication, said timer producing a timer value indicative of said elapsed time interval;

spreading timing controlling means, connected to said spreading code and spreading timing memory means, for generating spreading timings in consideration of the spreading timing stored in said spreading code and spreading timing memory means and a timing offset between sectors; and

known signal replica generating means connected to said timer, said spreading code and spreading timing detecting means, said spreading code and spreading timing memory means, and said delay profile calculating means, said known signal replica generating means making said delay profile calculating means generate a delay profile only near to the spreading timing stored in said spreading code and spreading timing memory means when said timer value is less than a first communication stop time interval threshold value on staring of a re-communication, said known signal replica generating means making said delay profile calculating means carry out a cell search processing near to the spreading timings generated by said spreading timing controlling means when said timer value is not less than said first communication stop time interval threshold value and is less than a second communication stop time interval threshold value on starting of the re-communication, said known signal replica generating means supplying said known signal replicas for N codes to said delay profile calculating means to make a normal cell search processing carry out when said timer value is not less than said second communication stop time interval threshold value on starting of the re-communication.

3. A cell search circuit for use in a code division multiple access (CDMA) system, comprising:

delay profile calculating means for, in a normal state, generating, by using known signal replicas for N codes, N delay profiles from a in-phase component signal and a quadrature component signal of a perch channel that are orthogonal detected and modulated, where N represents a positive integer which is not less than two, said delay profile calculating means producing a delay profile signal indicative of said N delay profiles;

spreading code and spreading timing detecting means, connected to said delay profile calculating means, for detecting, in response to said delay profile signal, a using spreading code and a using spreading timing by